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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,961	12/05/2001	Jason G. Sandri	2207/12035	1389
23838	7590	09/29/2006	EXAMINER	
KENYON & KENYON LLP 1500 K STREET N.W. SUITE 700 WASHINGTON, DC 20005			TRUONG, CAMQUY	
			ART UNIT	PAPER NUMBER
			2195	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/001,961	Applicant(s) SANDRI ET AL.	
	Examiner Camquy Truong	Art Unit 2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 20 July 2006.  
 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-17 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☐ All b) ☐ Some \* c) ☐ None of:  
 1. ☐ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input checked="" type="checkbox"/> Other: <u>Microsoft Dictionary P. 355</u>        |

### **DETAILED ACTION**

1. Claims 1-17 are presented for examination.
2. It is noted that although the present application does contain line numbers in the specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning with line 1. For ease of reference by both the examiner and Applicant all future correspondence should include the recommended line numbering.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
4. Claims 1-12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of Forman et al (5,544,353).
5. Hays and Forman were cited in the last office action.

6. As to claim 1, Hays teaches the invention substantially as claimed including: a method for controlling access to resources shared among a plurality of processors (1-2, Fig.1; col.1, lines 60-67), comprising

obtaining exclusive access for said first logical processor to said resource file if said lock is obtained (col.5, lines 32-37);

Query resource descriptor to determine whether resources needed by said first processor is available (col.4, lines 24-27; col.5, lines 32-35; col. 10, lines 20-21);

If resources needed by said first processor are available, updating said resource descriptor to reserve said resources for exclusive use by said first processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27); and

Releasing said exclusive access for said first processor to said resource descriptor (col. 10, lines 29-45).

7. Hays does not explicitly teach for a first logical processor, obtaining a lock on a semaphore controlling exclusive access to a resource descriptor if said lock is obtained, the resource descriptor describing a usage allocation of said shared resources.

However, Forman teaches obtaining a lock on a semaphore controlling exclusive access to a resource descriptor if said lock is obtained (if access denied (resource file is locked and access by other processor, waiting and retrying until exclusive access to file is obtained, col. 6, lines 9-11. It obvious that it using the semaphore method to control and allow accessing to share resource file one at the time), and the resource descriptor

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describing a usage allocation of said shared resources (col. 2, lines 33-41; col. 5, lines 3-9; col. 6, lines 3-10).

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Hays and Forman because Forman's obtaining exclusive access for a first processor to a resource descriptor describing a usage allocation of said shared resources would increase the efficiency of Hays's system by providing the step of obtaining exclusive access for a first processor to a resource descriptor describing a usage allocation of said shared resources to improve the efficiency using the share resource a among a plurality of logical processors.

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Hay, Forman, and Murata because Murata's obtaining a lock on a semaphore controlling exclusive access to a resource descriptor, and obtaining exclusive access for said first logical processor to resource descriptor if said lock is obtained would allow to access to the file one at the time by checking the lock before access to the file descriptor.

10. As to claim 2, Hays teaches if said resources needed by said first logical processor are not available, releasing said exclusive access for said first logical processor to said resource descriptor (col.5, lines 57-66).

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11. As to claim 3, Hays teaches after the releasing, accessing a shared resource by said first logical processor (col. 10, lines 39-45).

12. As to claim 4, Hays teaches:

Query resource descriptor to determine whether resources needed by said second logical processor is available (col.4, lines 24-27; col.5, lines 32-35; col. 10, lines 20-21);

If resources needed by said second processors are available, updating said resource descriptor to reserve said resources for exclusive use by said second processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27);

Releasing said exclusive access for said second processor to said resource descriptor (col. 10, lines 29-45); and

Forman teaches obtaining access for a second processor to a resource descriptor describing a usage allocation of said shared resources (col. 2, lines 33-41; col. 5, lines 3-9; col. 6, lines 3-10).

13. As to claim 5, Hays teaches if said resources needed by said second logical processor are not available, releasing said exclusive access for said second logical processor to said resource descriptor (col.5, lines 57-66).

14. As to claim 6, Hays teaches the invention substantially as claimed including: a method for controlling access to resources shared among a plurality of processors (1-2, Fig.1; col.1, lines 60-67), comprising

Writing to said resource descriptor register to reserve at least a first resource of said plurality of shared resources for exclusive use by said first logical processor (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27).

Forman teaches:

writing to a semaphore register to reserve access by a first logical processor to a resource descriptor register (col. 2, lines 33-41; col. 5, lines 3-9; col. 6, lines 3-10); and writing to semaphore register to release said exclusive access by said first logical processor (col. 6, lines 52-56).

15. As to claim 7, it is rejected for the same reason as claim 6. In addition, Hays teaches the second processor (1-2, Microprocessor A, Microprocessor B, Fig.1).

16. As to claim 8, Hays teaches resource descriptor register comprises at least one logical processor identifier associated with one of said first and second logical processors (col. 2, lines 20-21; col. 6, line 66-col.7, line 4).

17. As to claim 9, Hays teaches said resource descriptor register further comprises a status identifier associated with said logical processor identifier (col. 2, lines 20-23; col. 6, lines 3-11).

18. As to claim 10, Hays teaches:

A plurality of logical processors (1-2, Multiprocessor A, Multiprocessor B, Fig.1, col. 1, line 64);

A plurality of resources shared by said plurality of logical processors (col. 1, lines 59-64);

A resource descriptor to identify a status of said shared resources (col. 10, lines 9-13); and

A semaphore to control access by said plurality of logical processors to said resource descriptor (col. 2, lines 8-12; col. 10, lines 16-19).

19. As to claim 11, it is rejected for the same reason as claim 6.

20. As to claim 12, it is rejected for the same reason as claim 11. In addition, Hays teaches first and second processors concurrently use first and second resources (col. 1, lines 7-16; col. 7, lines 55-61).

21. As to claim 16, it is rejected for the same reason as claim 6. In addition, Hays teaches:

A plurality of processors and plurality of resources shared by said processor (1-2, Multiprocessor A, Multiprocessor B, Fig.1, col. 1, lines 59-64);

A resource descriptor that controls access to said resources (col.2, lines 9-12; col.10, lines 10-13 and 16-19);



A semaphore register that controls access to said resources descriptor (col. 2, lines 8-12; col. 10, lines 16-19);

A semaphore access control hardware that controls access to said semaphore register (col. 2, lines 8-12; col. 10, lines 16-19);

Causing a first logical processor to execute software to supply an identifier of said first logical processor to said semaphore access control hardware (col. 2, lines 20-21).

22. Claim 17 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of Forman et al (5,544,353), and further in view of Scalzi et al (U.S. Patent 5,895,494).

23. Scalzi was cited in the last office action.

24. As to claim 17, it was rejected as claims 6 and 16 above, in addition. Hays teaches: Causing a first logical processor to execute software to supply an identifier of said first logical processor to said semaphore access control hardware (col. 2, lines 20-21).

25. Hays does not explicitly teach writing said identifier to semaphore register to release said exclusive access by said first logical processor. However, Forman teaches writing said identifier to semaphore register to release said exclusive access by said first

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logical processor (col. 2, lines 7-10, and lines 33-41; col. 3, lines 15-18; col. 5, lines 3-9; col. 6, lines 3-10; and lines 53-57).

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays and Forman because Forman's writing to a semaphore register to reserve/ release access by a first logical processor to a resource descriptor register would improve the book keeping of resources for a multiprocessor system by explicitly having the processor to write to the register when reserve/release the resources.

27. Hays and Forman do not explicitly teach that detecting said first logical processor has failed. However, Scalzi teaches detecting said first logical processor has failed (col. 4, lines 1-7; col. 7, lines 42-44; col. 8, lines 9-14).

28. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hays, DeKoning and Scalzi because Scalsi's detecting said first logical processor has failed would improve the data integrity of Hays and Dekoning's system with relative ease when any processor fails during its execution of a Perform Locked Operation.

29. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable Hays, Jr. et al. (U.S. Patent 4,354,227) in view of Forman et al (5,544,353), and further in view of Florek (U.S. Patent 6,795,901).

30. Florek was cited in the last office action.

31. As to claim 13,

Hays teaches:

Generating a first bitmap identifying said first required resource (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27), and using first resource (col.10, lines 43-45);

Applying said first bitmap to said resources descriptor register to reserve said first require resource (col. 5, lines 35-36; col. 6, lines 3-6; col. 10, lines 22-27).

Hay does not explicitly teach setting a lock bit in a semaphore register to reserve exclusive access to resource descriptor register; and re-setting semaphore lock bit to release exclusive access. However, Forman teaches setting a lock bit in a semaphore register to reserve exclusive access to resource descriptor register (write a master process identification information, wherein each processes having a separate address space, to share resources control file, col. 2, lines 33-41; col. 3, lines 15-18; col. 5, lines 3-9; col. 6, lines 3-10); and re-setting semaphore lock bit to release exclusive access (col. 2, lines 7-10; col. 6, lines 53-57).

32. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Hays and Forman because Forman's setting a lock bit in a semaphore register to reserve exclusive access to resource descriptor register, and re-setting semaphore lock bit to release exclusive access would increase the efficiency of Hays's system by setting a lock bit in a semaphore register to reserve exclusive access to resource descriptor register to improve the efficiency using the share resource a among a plurality of logical processors.

33. As to claim 14, it is rejected for the same reason as claim 13. In addition, Hays teaches first and second processors use first and second resources in parallel (col. 1, lines 7-16; col. 7, lines 55-61).

34. As to claim 15, Hays teaches setting a lock bit comprises supplying an identifier of said first logical processor for writing into said semaphore register (col. 2, lines 20-21; col. 6, lines 3-11; col. 6, line 66-col.7, line 4).

### ***Response to the argument***

35. Applicant arguments filed on 7/20/06 had been considered but they are not persuasive. In the remarks applicant argued (1) Forman does not disclose obtaining a lock on a semaphore that controls access to a resource descriptor, and if the lock is obtained, obtaining exclusive access to the resource descriptor.

36. Examiner respectfully traverses Applicant's remarks:

As to point (1), Forman explicitly teaches obtaining a lock on a semaphore controlling exclusive access to a resource descriptor if said lock is obtained (if access is denied (resource file is locked and access by other processor), waiting and retrying until exclusive access to file is obtained, col. 6, lines 9-11). It is obvious that it using the semaphore method to control and allow accessing to share resource file one at the time).

In addition, Forman teaches requesting exclusive access to a share resource file, if access is denied, waiting and retrying until exclusive access to file is obtained (col. 6, lines 9-11). It is well known to those skilled in the art that exclusive access to the share resource file that allow one program or routine at a time can access some resource (for example: Computer Dictionary, Fifth Edition, disclose mutual exclusion is a programming technique the ensures that only one program or routine at a time can access some resource). Therefore, it has been obvious that Forman teaches exclusive lock. Then, Forman teaches if the lock is obtained, allow to access to the share resource file.

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


### ***Conclusion***

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Camquy Truong whose telephone number is (571) 272-3773. The examiner can normally be reached on 8AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3756.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Camquy Truong

  
MENG-AI T. AN  
SUPERVISORY PATENT EXAMINER  
TECHNICAL CENTER 219



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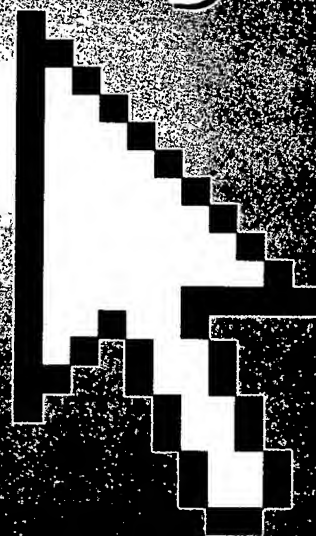
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multum in parvo mapping

shared by several people can be considered a multiuser system, the term is generally reserved for machines that can be accessed simultaneously by several people through communications facilities or via network terminals. Compare single-user computer.

**multum in parvo mapping** *n.* See MIP mapping.

**MUMPS** *n.* Acronym for Mass(achusetts) Utility Multi Programming System. An advanced, high-level programming language and integrated database developed in 1966 at Massachusetts General Hospital and used widely by health care businesses. A unique feature of MUMPS is its ability to store both data and program fragments in its database.

**munging** *n.* See address munging.

**MUSE** *n.* Short for multiuser simulation environment. See MUD.

**.museum** *n.* One of seven new top-level domain names approved in 2000 by the Internet Corporation for Assigned Names and Numbers (ICANN), .museum is meant for use by museum Web sites.

**Musical Instrument Digital Interface** *n.* See MIDI.

**mutual exclusion** *n.* A programming technique that ensures that only one program or routine at a time can

my two cents

access some resource, such as a memory location, an I/O port, or a file, often through the use of semaphores, which are flags used in programs to coordinate the activities of more than one program or routine. See also semaphore.

**MUX** *n.* See multiplexer.

**My Briefcase** *n.* A Windows 9x utility, helpful for workers away from the office, that manages the updating of modified files once the remote user's computer is connected back on the office network.

**Mylar** *n.* A polyester film product created by DuPont, often used as the base for magnetically coated storage media (disks and tape) and for carbon ribbons used with impact printers.

**Mylar ribbon** *n.* See carbon ribbon.

**MYOB** *n.* Acronym for Mind your own business. An expression used in e-mail and newsgroups.

**my two cents** *n.* An expression used informally in newsgroup articles and, less frequently, e-mail messages or mailing lists, to indicate that the message is the writer's contribution to an ongoing discussion. Also called: \$0.02. See also mailing list, newsgroup.

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